

FIG. 20A

PRIOR ART

The diagram illustrates a prior art circuit configuration. It features three main blocks: 101 (top right), 106 (left), and 110 (bottom right). Block 101 contains a CMOS inverter (10) with input IN and output OUT, powered by VDD1 and VSS1. Block 106 contains a CMOS inverter (10) with input IN and output OUT, powered by VDD2 and VSS2. Block 110 contains a pass transistor (112) and a CMOS inverter (113) powered by VDD3 and VSS3. The output OUT of block 106 is connected to the input of block 110. A vertical line 115 represents a signal line. The output OUT of block 101 is connected to line 115. The pass transistor 112 is connected between line 115 and the input of inverter 113.

The diagram shows a square wave signal for VDD1 OR VDD2 and a constant low signal for VSS1 OR VSS2. The VDD1 OR VDD2 signal is a square wave that transitions between high and low states. The VSS1 OR VSS2 signal is a constant low signal.

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